

## Paper TP6.5: 128 Mbit/second Multiport CMOS Binary Active Pixel Image Sensor

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A 128 x 128 photo-diode active pixel sensor (APS) with an on-chip array sequencing controller and 1 bit thresholding circuitry was designed to process 8,192 frames per second at a 128Mbit data rate onto a 8 bit wide parallel digital output port. In addition, the on-chip controller can be commanded to output data through either a serial digital port for lower bandwidth requirements or through a serial analog port for higher resolution off-chip analog to digital conversion.

The sensor chip development is for a real-time helicopter oil debris monitoring system requiring the sensing and processing of 1,024 laser-strobed snapshot images per second of oil flowing through a transparent tube in the operating engine. The light exiting the tube opposite the laser source is projected onto the sensor leaving shadows where particles (e.g. metal chips or sand) in the oil obstruct the passage of light. Because of the high contrast nature of the image, the analog pixel data is converted to only a 1 bit digital representation. This binary pixel data is sent off chip to a set of parallel processors performing particle discrimination.

Greek letter  $\mu$  →  $\mu$  = mu used for "1 micro-meter N-well" → The 4.3mm x 4.5mm image sensor is fabricated in a 1  $\mu$ m N-well standard CMOS process, and all sensor array control and readout electronics are implemented on-chip. In each of the 128 x 128 active pixels there is a photo-diode for collecting electrons generated by the laser source, a source follower for buffering the photo-diode, a selection transistor for enabling the pixel's source follower, and a transistor for resetting the photo-diode. The pixel contains only N-channel transistors and is similar to previously reported pixel designs'. The photo-diode is formed between a n<sup>+</sup> diffusion and the p type substrate. For this process the pixel is 16 x 16  $\mu$ m<sup>2</sup> or 310/0 of the pixel area is occupied by the photo-diode n<sup>+</sup> diffusion. ← superscript reference 1

Greek letter  $\mu$  →  $\mu$  = mu used for "16x 16 micro-meter" →

As shown in the chip block diagram in figure 1, the active pixel array contains 128 rows and 128 columns (16K pixels). When a row is selected, active pixels in that row output data onto a shared

column output through the pixel source follower. The datapath for a single pixel is shown in figure 2. A pointer in the vertical 128 bit shift register (figure 1) preloaded with a 1 is used by logic in each row to select a row of pixels and enable pixel reset for that row. For the digital output ports, per column output circuitry at the bottom of the array clamps pixel output data onto a capacitor and compares it to an externally applied threshold voltage (figure 2). This thresholded pixel data is loaded into a register. The time for accessing a row of pixels, sampling the column

Greek letter →  
 $\mu$  = mu used  
 for "1 micro-  
 second"

onto the clamping capacitor, and performing the comparison is 1  $\mu$ sec. The on-chip controller in the lower left of figure 1 then selects a byte at a time from the register for readout onto the 8 bit 16 MHz parallel data output bus. To read out all 128 bits from the register requires 16 internal clock cycles for a total time of 1  $\mu$ sec at a 16 MHz clock rate. In serial mode, the controller enables the register to shift the digital data out serially. As data from the register is read out, the next row in the array is being processed by the per column 1 bit conversion circuitry. In this pipelined process as the last of the bits from the register are read out, this next set of thresholded data is loaded. To read out all 128 rows of the array in the parallel

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 for "1 micro-  
 second"

Greek letter →  
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 for "128 micro-  
 second"

port output mode requires 128  $\mu$ sec (8 KHz frame rate).

For the analog output ports, per column output circuitry at the top of the array clamps the pixel output data onto a capacitor that is connected to the gate of a source follower (figure 2). A shift register located above the source follower selects the individual columns for readout through the analog port.

The on-chip control logic performs the array timing for the three separate modes of operation for the three different ports. Two chip inputs set the readout mode of operation. In addition, there are control inputs to reset the control logic (to put the sensor into a known state at power up), a chip enable control to make the sensor pause between frames (not normally used), and a 16 MHz clock. On-chip logic state machines sequence the array to generate the output data and control flags. The control flags signal the start of a frame and a row and also identify when the output data is valid. A signal is also generated at the end of a frame to command the laser to generate a pulse. Digital timing and control functions plus digital control for row/column circuitry comprise approximately 29,500 transistors as shown in table 1.

The analog output port was used to characterize the pixel array (table 1). The low sensor quantum efficiency is a factor of 4 to 5 times smaller than previous designs due to an opaque silicide on the photo-active n+- implanted regions (figure 3). The maximum output response on the analog output port is 1.2V. Because there is no column-wise fixed pattern noise (FPN) suppression circuitry, approximately 30 mV p-p of variation in analog output signal exists across the array for uniform illumination.

Images at a 301 Hz frame rate from the serial analog port and parallel digital port are shown in figures 4,5. At video rate speeds the sensor's three separate output modes functioned as expected. However, at much higher frame rates the parallel digital output mode produced interline noise coupling which is believed to come from output pad - substrate coupling.

To avoid digital output driver noise from coupling back into the comparator circuitry, the timing and control logic should be designed to disable the output drivers during the sensitive 1-bit thresholding operation. To offset the reduced time to readout the digital data from the chip due to this break in the pipelined sensor readout, the output bus bandwidth can be increased.

#### *Acknowledgment*

The research described in this paper was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the Naval Research Laboratory (NRL), through an agreement with the National Aeronautics and Space Administration. The authors appreciate the encouragement of Dr. John Reintjes of NRL.

#### *References*

<sup>1</sup>S. Mendis, S.E. Kemeny, R. Gee, B. Pain, and E.R. Fossum, *Progress in CMOS active pixel image sensors*, in Charge-Coupled Devices and Solid State Optical Sensors IV, Proc. SPIE vol. 2172, pp. 19-29 (1994).

Figure 1: Multiport CMOS binary APS block diagram

Figure 2: Circuit diagram of pixel datapath

Table 1: Multiport AI'S sensor characteristics

Figure 3: Absolute quantum efficiency of sensor

Figure 4: Serial analog port data

Figure 5: Digital parallel port data

Figure 6: Photograph of 128 Mbit/second Multiport CMOS Binary APS Sensor

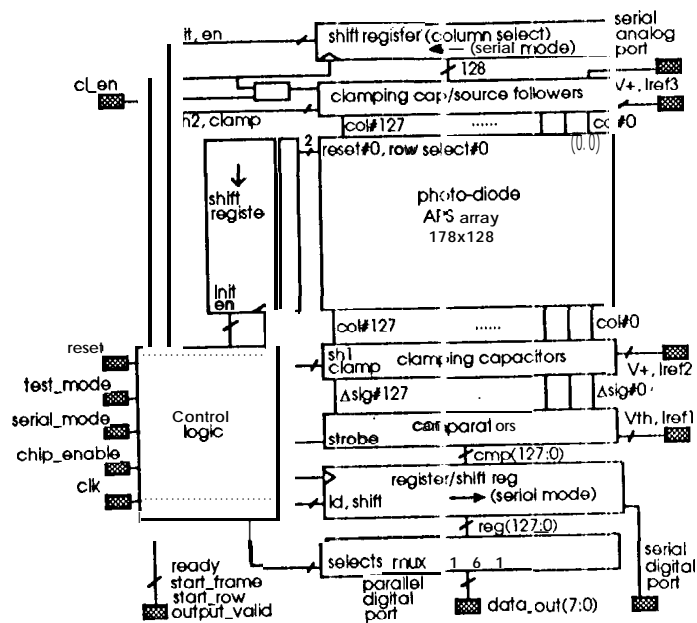


Figure 1: Multiport CMOS binary APS block diagram.  
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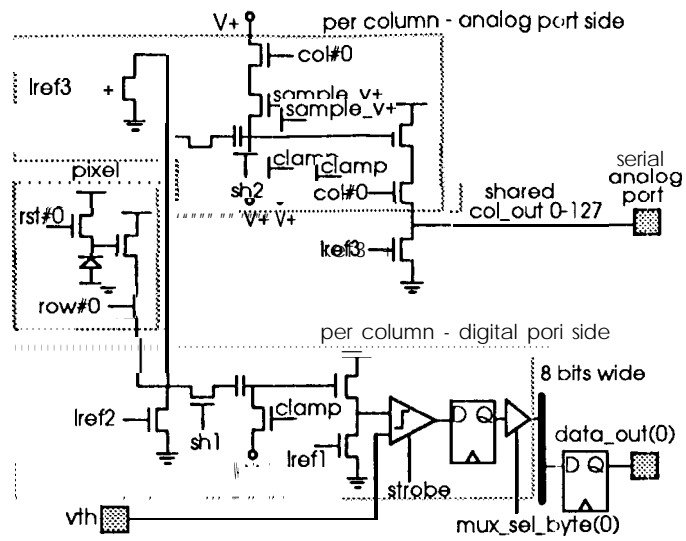


Figure 2: Circuit diagram of pixel datapath.  
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Measurement	Result
Conversion Gain	2.34 $\mu\text{V}/\text{e}^-$
Quantum Efficiency @ 660 nm	0.12
Dynamic Range	70.8 dB
Saturation	1.2 V
Dark Rate	9.3 mV/s
Fixed Pattern Noise	29.7 mV
Fixed Pattern Noise, % of Saturation	2.48 %
Number of Transistors:	
digital logic	29,518
analog circuits	3,983
pixel array	49,152
Total	82,653
Power: 5V supply	
analog mode (13.6 Hz frame rate)	32 mW
digital mode (1.5 KHz frame rate)	100 mW

Table 1: **Multiport** APS image sensor characteristics.  
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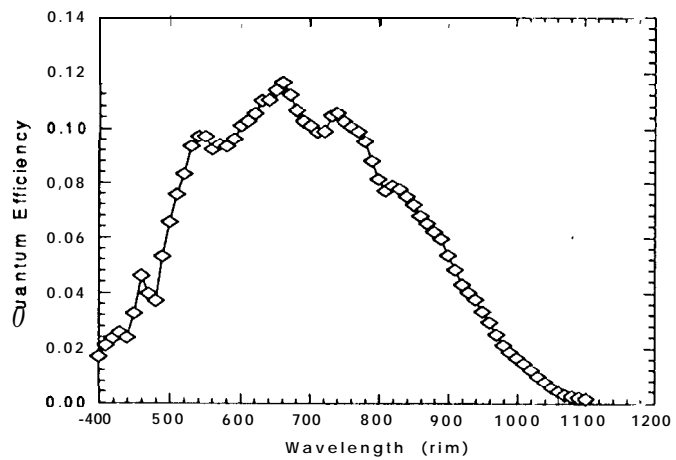


Figure 3: Absolute quantum efficiency of sensor.  
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Figure 4: Serial analog port data.  
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Figure 5: Digital parallel port data.  
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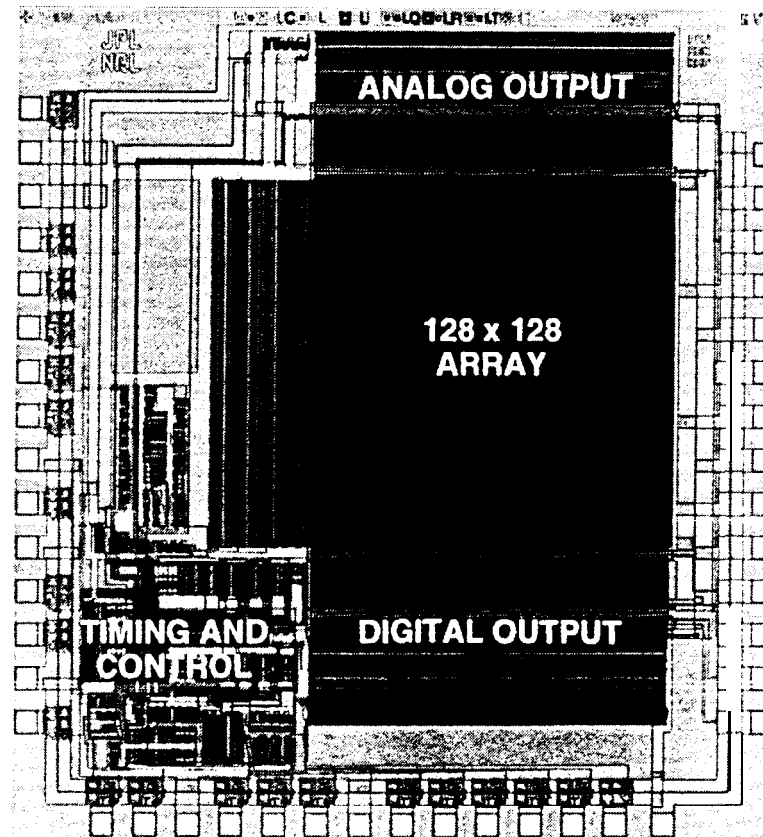


Figure 6: Photograph of 128 Mbit/second Multiport CMOS Binary APS Sensor  
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